Ashiqur Rasul

ECE Ph.D. Student Specializing in Hardware-Software Co-design

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EDUCATION

- **PhD in Electrical and Computer Engineering** — *Aug 24 – Present*
  Georgia Institute of Technology — *CGPA - 4.00/4.00*
  Research Thesis Topic: *Hardware Software Co-design for Adaptive and Compute Efficient ML Workload.*
- **M.Sc. in Electrical and Computer Engineering** — *Aug 24 – Dec 25*
  Georgia Institute of Technology — *CGPA- 4.00/4.00*
- **B.Sc. in Electrical and Electronics Engineering** — *Feb 17 – May 22*
  Bangladesh University of Engineering and Technology — *CGPA- 3.89/4.00*

RELEVANT PROFESSIONAL EXPERIENCE

- ***Graduate Research Assistant, Georgia Institute of Technology*** — *Jan 25 - Present*
  Low Power, Adaptive and Resilient Systems (LARS), PI: Dr. Abhijit Chatterjee
- ***Lecturer, Bangladesh University of Engineering and Technology*** — *Nov 22 – Aug 24*
  Department of Electrical and Electronic Engineering

SELECTED PUBLICATIONS

1. **Ashiqur Rasul,** Abhijit Chatterjee, "ACE: Adaptive Compute-Efficient State Space Models with Dynamic Token Routing", *AAAI 2026(under review)*- Studies the prospect of dynamic token skipping in Mamba state space model, where semantically insignificant tokens are routed past compute-heavy SSM blocks and experiments show that half of the tokens can be skipped with no performance degradation while improving inference throughput.
2. **Ashiqur Rasul**, Anurup Saha, Sai Pranav Komaragiri, Abhijit Chatterjee, "CASPER: Confidence-Guided Adaptive Nearest Neighbor Search with In-DRAM Processing for Efficient Information Retrieval", *Design Automation and Test in Europe (DATE), 2027 (under review)* - Introduces the notion of dimension adaptivity in retrieval augment generation and adopts in-DRAM computing architecture to parallelize and accelerate hamming similarity matching between queries and documents, resulting in reduction of memory accesses and around 10× speedup compared to GPU.
3. Anurup Saha, **Ashiqur Rasul**, Thomas Walton, Amirali Aghazadeh, Abhijit Chatterjee, "Adaptive Testing of Compute-in-Memory GANs Using Backpropagation-Guided Test Compaction", *Design Automation and Test in Europe (DATE) 2026* – Investigates process variations on analog crossbar arrays for compute-in-memory architecture and proposes adaptive test framework that enables around 7× speedup during testing compared to exhaustive test sets.
4. Abhijit Chatterjee, Niraj Jha, Jonathan D. Cohen, Thomas L. Griffiths, Lu Hongjing, Diana Marculescu, **Ashiqur Rasul**, Keshab K. Parhi, "Energy-Efficient Domain Specific Artificial Intelligence Models and Agents: Pathways and Paradigms", *ACM Computing Surveys, 2025* – Envisions a shift from computationally expensive foundational models toward energy efficient and domain specific AI agents through cross-layer algorithm hardware co-design and brain-inspired computing.
5. Mohammed Mejri, **Ashiqur Rasul**, Abhijit Chatterjee, "Dynamic 3D CNN Pruning: Joint Frame, Channel, and Feature Adaptation for Energy Efficiency on the Edge", *CVPR Workshop, 2025* – Explores input-dependent, fine-grained pruning of 3D CNN models to reduce the number of active parameters in the computation graph and increase efficiency.

RESEARCH FOCUS

- Hardware-Software Codesign
- Hardware Acceleration
- Efficient Neural Network Architecture
- Adaptive Hardware Design for AI Acceleration

AWARDS AND HONORS

- Dean's List Scholarship, BUET (academic excellence at undergraduate level in each academic year), 2017 - 2022
- University Merit Scholarship, BUET (based on results of undergraduate study in each term), 2017-2022
- University Technical Scholarship, BUET, 2017 – 2022

RESEARCH/ACADEMIC PROJECT INVOLVEMENT

- Compute Efficient Recursive State Space Models – funded by NSF.
- Dynamic Quantization of Language Models with Implementation on Neuromorphic Computing Hardware – funded by NSF
- Adaptive Activation Sparsity in Convolutional Neural Networks – funded by NSF.
- Development of Test Ordering Algorithm and BIST Framework for High-Speed Analog Circuits – funded by Semiconductor Research Corporation (SRC).
- Develop C++ Program for End-to-End Deductive Fault Simulation and Path Oriented Decision Making (PODEM) Framework – course project for Digital Systems Test.

TAPEOUT PROJECTS

- Design, Verification, Synthesis, Static Timing Analysis and Tapeout of a Systolic Array Processor with TSMC 65 nm PDK – course project for VLSI Design: Theory to Tapeout.
- Design, Verification, Synthesis, Tapeout and Characterization of Sparsity Enabled Diagonal Dataflow Systolic Array Architecture with TSMC 28 nm HPC PDK – research project funded by DARPA (ongoing).

TECHNICAL SKILLS

- **Programming Languages:**
  C++, CUDA, MPI, Verilog, SystemVerilog, Python, JAX, PyTorch, TensorFlow, Linux Scripting
- **Simulation Tools:**
  MATLAB, Quartus, Xilinx Vivado, National Instruments Labview
- **Design Tools:**
  Cadence Virtuoso, Spectre, HSpice, Synopsys Design Compiler (DC), IC Compiler II (ICC2), and PrimeTime

RELEVANT COURSEWORK

Advanced Computer Architecture | Physical Design Automation | DSP Hardware System Design | Gigascale Integration | Advanced Programming Techniques | Microprocessor and Interfacing | VLSI Design: Theory to Tapeout | Digital Systems Test